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ABSTRACT OF THE DISCLOSURE

Disclosed herein is a method comprised of providing a wafer comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, and a semiconducting layer positioned above the insulating layer, forming an opening in the semiconducting layer and the insulating layer to thereby expose a surface area of the bulk substrate, forming an alignment mark in the bulk substrate within the exposed surface area of the bulk substrate, and forming a layer of material above the alignment mark and in the opening. A wafer is also disclosed herein that is comprised of a bulk substrate, an insulating layer positioned above the bulk substrate, a semiconducting layer positioned above the insulating layer, an opening formed in the semiconducting layer and the insulating layer, an alignment mark formed in the bulk substrate within an area defined by the opening, and a layer of material positioned above the alignment mark and within the opening.